throughout the originally filed disclosure. Applicants submit that the present Amendment does not generate any new matter issue.

A clean copy of amended claim 13 appears in the Appendix hereto.

Clarification of the Record

Applicants note the Examiner acknowledged receipt of the Information Disclosure Statement (IDS) but only included a partially initialed copy of Form PTO-1449 indicating consideration of the references with the exception of the Japanese references. Applicants would request the Examiner to clarify the record by providing an appropriately initialed copy of Form PTO-1449 indicating consideration of each of the cited references, including the Japanese references. In this respect, Applicants would note that in the parent Application, the same Japanese references were considered by the Examiner.

Applicants would request the Examiner to further clarify the record by acknowledging that the November 20, 2002 Office Action erroneously refers to claims 11 through 13; whereas, claims 12 through 14 were pending. Applicants would clarify that by the present Amendment, claims 12 and 14, which appear to correspond to what the Examiner had previously viewed as claims 11 and 13, have been cancelled. Applicants would further clarify the record by noting that claim 13 has been amended, which apparently corresponds to what the Examiner had previously viewed as claim 12.

Claims 11 and 12 (presumably intending claims 12 and 13) were rejected under 35 U.S.C. §103 for obviousness predicated upon Todorobaru et al. in view of the acknowledged prior art.

In the statement of the rejection, the Examiner admitted that Todorobaru et al. do not disclose forming a contact hole reaching the second gate electrode. However, the Examiner asserted that one having ordinary skill in the art would have been motivated to modify the methodology disclosed by Todorobaru et al. by forming a contact hole and interconnection reaching a gate electrode, allegedly consistent with conventional practices as in the acknowledged prior art, pointing to Fig. 37B on pages 1 through 3 of the written description of the specification. As to claim 12 (presumably intending claim 13), the Examiner referred to Fig. 23 of Todorobaru et al. pointing to first metal silicide layer 35A and second metal silicide layer 35B at the surface of plug electrode 25. This rejection is traversed.

Firstly, this rejection has been rendered moot with respect to claim 12 (Examiner's claim 11), by cancelling claim 12. As to claim 13 (Examiner's claim 12) Applicants submit that there are significant differences between the claimed method and the methodology of Todorobaru et al., even in combination with the acknowledged prior art, that undermine the obviousness conclusion. Specifically, in accordance with the claimed method, the first and second metal silicides are formed through different manipulative steps. Not so with the methodology of Todorobaru et al. who require metal silicides 35A and 35B to be formed in the same step. This difference in manipulative steps is functionally significant. Specifically, in accordance with the present invention, since the

first and second metal silicides are formed utilizing different manipulative steps, the thickness of the metal silicides can be tailored or varied independently. However, in accordance with the methodology of Todorobaru et al., since metal silicides 35A and 35B are formed utilizing the same manipulative step, it is not possible to independently vary the thickness of the metal silicide 35A from that of metal silicide 35B.

It should, therefore, be apparent that even if the applied references are combined, as suggested by the Examiner, the claimed invention would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).* Further, there is no apparent factual basis upon which to predicate the conclusion that one having ordinary skill in the art would have been realistically motivated to modify whatever methodology can said to have reasonably been suggested by the combined disclosures of Todorobaru et al. and the acknowledged prior art to arrive at the claimed invention, absent improper reliance upon Applicants' disclosure. *Panduit Corp. v. Dennison Mfg. Co., 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985).*

Applicants, therefore, submit that the imposed rejection of claim 13 (Examiner's claim 12), noting that claim 11 (Examiner's claim 12) has been cancelled, under 35 U.S.C. §103 for obviousness predicated upon Todorobaru et al. in view of the acknowledged prior art is not factually or legally viable and, hence, solicit withdrawal thereof.

Claim 13 (presumably intending claim 14) was rejected under 35 U.S.C. §103 for obviousness predicated upon Todorobaru et al. in view of Kim et al.

This rejection has been rendered moot by cancelling claim 14 (Examiner's claim 13).

It should, therefore, be apparent that the imposed rejection of claim 13 (Examiner's claim 12) has been overcome. As claim 13 (Examiner's claim 12) is the only pending claim, Applicants submit this application is in clear condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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REMARKS

Claim 13 now reads as follows.

13. (Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming first and second transistors on a main surface of a semiconductor substrate with a space between each other;

forming first metal silicide at a surface of a source/drain of said second transistor with a source/drain of said first transistor being covered by an insulating film;

forming an interlayer insulating film covering said first and second transistors;

forming in said interlayer insulating film a first contact hole reaching one of said source/drain of said first transistor;

forming a plug electrode in said first contact hole;

forming in said interlayer insulating film a second contact hole reaching one of said source/drain of said second transistor;

forming second metal silicide on said plug electrode; and

forming a bit line on said second metal silicide and an interconnection in said second contact hole.

Claims 12 and 14 have been cancelled.